

SDIF-3

Version 1.0

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Sony Corporation

1. Purpose

The purpose of SDIF-3 format digital interface is to enable DSD signal exchange between various DSD equipment.

2. Application area

SDIF-3 format digital interface is to be used as DSD signal exchange between DSD equipment.

3. Overview

This interface is based upon 75ohm BNC, unbalance transmission, 1channel in one cable and external word clock(WCK). And its bit rate is 5.6448MbPS(fsd = 2.8224Mbps) or 11.2896Mbps(fsd = 5.6448Mbps). Transmission is 1channel unbalance transmission and it uses word clock as synchronization technique.

4. Physical Characteristics

The SDIF-3 interface is based upon connectors and cables generally covered by the description "75ohm BNC".

An equipment output is presented on a single 75ohm BNC female connector. If the equipment has a conducting/metallic chassis the outer conductor of the BNC connector shall be directly bonded to the chassis.

An equipment input is presented on a single 75ohm BNC female BNC connector, If the equipment has a conducting/metallic chassis the outer conductor of each BNC connector shall be directly bonded to the chassis. Provision should be made to provide a switchable 75ohm termination at each receiver. Such switching may be accomplished, either physically or electrically, locally or remotely, manually or automatically.

5. Logical Characteristic

5-1 Modulation Method.

Phase Modulation

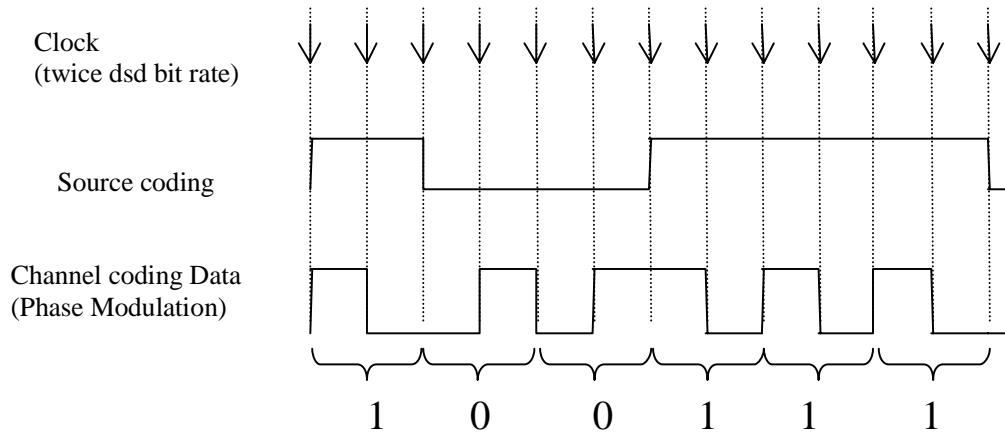
Bit rate= 5.6448Mbps when fsd is 2.8224MHz.
=11.2896Mbps when fsd is 5.6448MHz.

5-2 Word Clock

Duty 50%(±10%) frequency=44.1kHz

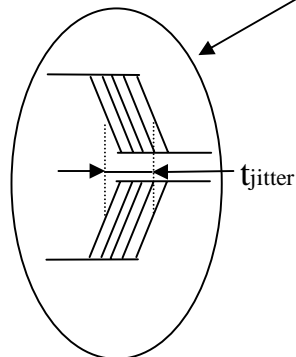
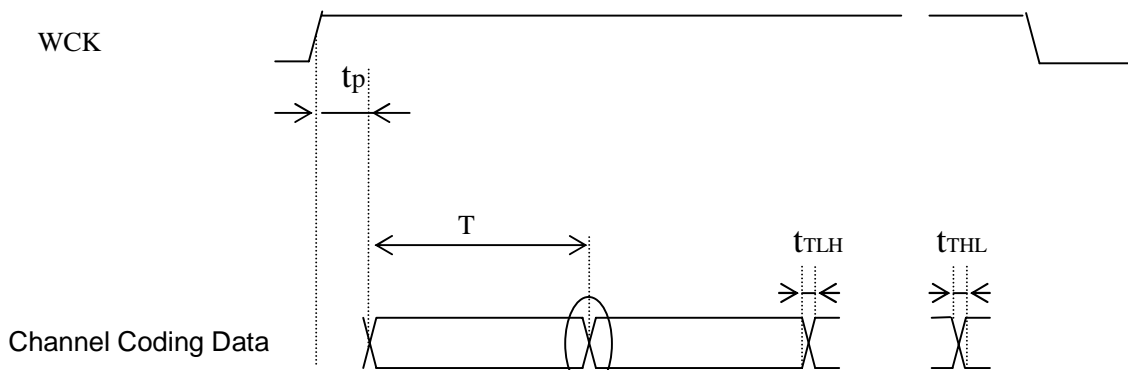
5-3 Format

It consists of signals of data and Word Clock , and data bits are immediately followed by their inverted bit signals.



6. Timing Chart

Word Clock(WCK) and Channel coding data timing.

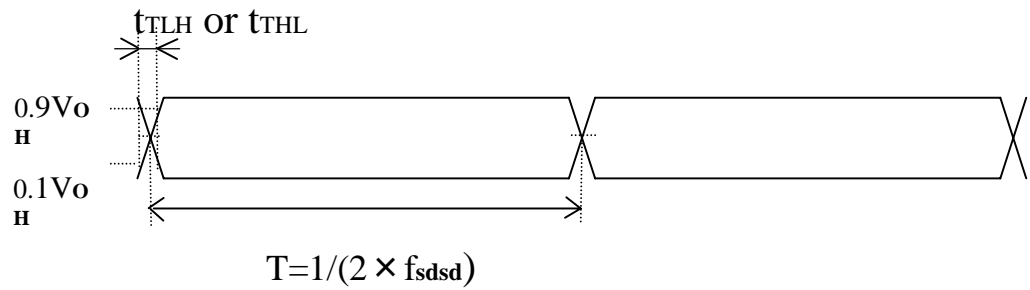


| Parameter | |
|-----------------------------|--|
| T | $T = 1/(2 \times f_{dsd})$ (typical) |
| t_p | $-20 \text{ ns} < t_p < 20 \text{ ns}$ |
| t_{TLH} (Rise Time) | $t_{TLH} < 10 \text{ ns}^{*1}$ |
| t_{THL} (Fall Time) | $t_{THL} < 10 \text{ ns}^{*1}$ |
| t_{jitter} (peak to peak) | $t_{jitter} < 5 \text{ ns}$ |

^{*1}When cable length=0m and 75Ω terminated.

$t_{TLH} = t_{THL}$ is desirable.

V_{OH} (Output Voltage High)



7. Electrical characteristic

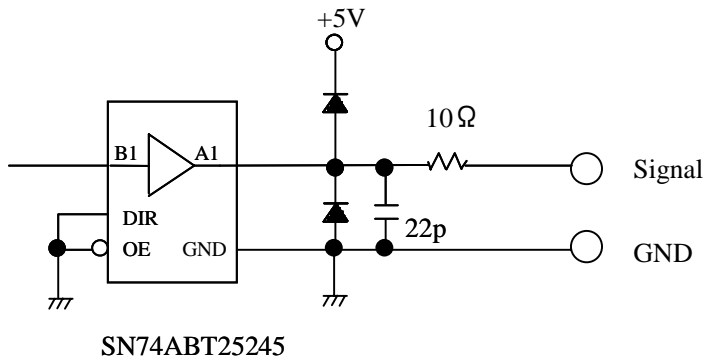
| Parameter | |
|-----------|--------------------------------|
| V_{OH} | $V_{OH} > 2.4V$ ^{*2} |
| V_{OL} | $V_{OL} < 0.55V$ ^{*2} |

^{*2} When cable length=0m and 75 Ω terminated.

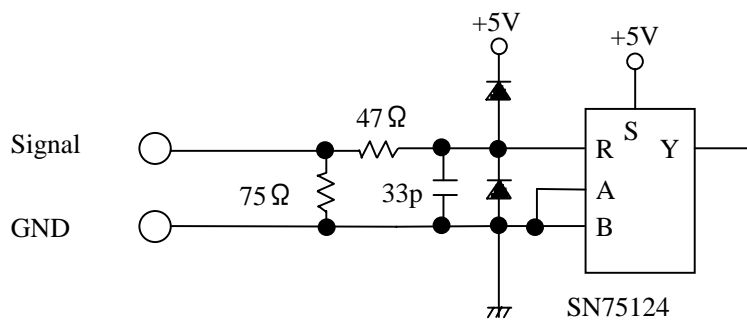
8. Appendix

A. Recommended circuit diagrams

A-1 Unbalanced Driver



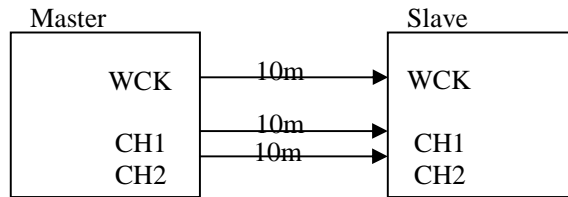
A-2 Unbalanced Receiver



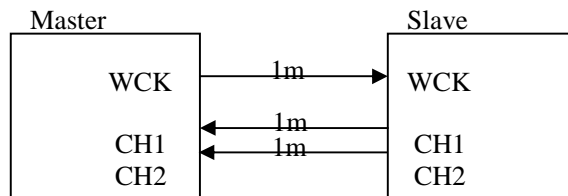
APPENDIX

As SDIF-3 format DIO interface sends WORD CLOCK and DATA in different BNC cable, there can be a difference in delay time between them. And also as SDIF-3 DATA is 88.5ns period high-speed signal, there is a possibility of bit shift of data. Consideration on selection of BNC cable and connection is needed to avoid this data bit shift.

1. When data transmitter is WORD CLOCK master.



2. When data receiver is WORD CLOCK master.



3. When there is a WORD CLOCK distributor.

